PTO/SB/08A (10-98)
Approved for use through 10/31/99. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known	
Application Number	10/768,558
Filing Date	January-29, 2004
First Named Inventor	Christopher Hamlin
Group Art Unit	2825
Examiner Name	S. Whitmore
Attorney Docket No.	103-2099

Sheet 1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number	Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AW		20020059054		Bade et al.	05-16-2002	
AW		20030005401		Shmuel Wimer	01-02-2003	
AW		5,500,805		Lee; Ven L. (Los Altos Hills,	03-19-1996	
		5,563,801		Cheung; Cyrus C. (Hercules,	06-10-2003	
		5,754,826		Gamal; Abbas El (Palo Alto,	05-19-1998	
		6,102,961		Lee et al.	08-15-2000	
		6,219,819		Vashi et al.	04-17-2001	
		6,625,788		Vashi et al.	09-23-2003	
		6,757,882		Bym et al.	06-29-2004	
AW		6,871,154		Bym et al.	03-22-2005	

Best Available Copy

Examiner signature	AW	Date considered	8/3/05

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office.

1/29/04

In Place of FORM PTO-1449 (Modified)	Serial No.:
	Applicant: Christopher Hamlin, et al.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Filing Date: January 29, 2004
	Group:
	Atty. Docket No.: 03-2099
	EXAMINER NAME: S. Whitmore

Reference Designation

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

AAA "Layout Compaction Accelerates SoC Design Through Hard IP Reuse," by Coby Zelnik, Senior Vice President, Business Development, Sagantec, Fremont, California, EE Times December 19, 2002 (10:47 a.m. EST); 3 pages; http://www.eetimes.com/story/OEG20021219S0026.

ABA "Layout Compaction in Digital Circuits," by Prof. Kurt Keutzer and A.R. Newton, EECS, University of California, Berkeley, CA; Implication of Deep Submicron, Simplex Solutions; © 1997, A. Richard Newton; 16 pages; www-cad.eecs.berkeley.edu/HomePages/keutzer/classes/ee244fa98/lectures/ee2443_2/ee2443_2.pdf.

ACA "Layout Compaction for Yield Optimization Via Critical Area Minimization," by Youcef Bourai and C.-J. Richard Shi, Electrical Engineering Department, University of Washington, Box 352500, Seattle, Washington 98195; 4 pages; http://jamaica.ee.pitt.edu/Archives/ProceedingArchives/Date/Date2000/papers/2000/date00/pdffiles/02c_4.pdf.

ADA "VLSI Layout Compaction Using Radix Priority Search Trees," by Andrew J. Harrison, March 12, 1991; 5 pages; Http://www.sigda.org/Archives/ProceedingArchives/Dac/Dac91/papers/1991/dac91/41_4/41_4.htm.

AEA "New Algorithms for Minimizing the Longest Wire Length During Circuit Compaction," by Susanne E. Hambrusch, Department of Computer Sciences, Purdue University, West Lafayette, IN 47907 and Hung-Yi Tu, Department of Computer Science and Information Management, Providence University, Taichung, Taiwan, ROC; January 26, 1995; 33 pages; http://www.cs.purdue.edu/homes/seh/papers/long-jour.pdf.

AFA "A Graph Based Simplex Method for the Integer Compaction Problem," by Alexey Lvov and Fook-Luen Heng, IBM Research; 1 page; http://researchweb.watson.ibm.com/compsci/algorithms/seminar.html.

AGA "Layout Synthesis Techniques for Yield Enhancement," by Venkat K.R. Chiluvuri and Israel Koren, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, MA 01003; 21 pages; http://citeseer.ist.psu.edu/cachedpage/90278/1. Originally published in *IEEE Trans. on Semiconductor Manufacturing*, Vol. 8, Special Issue on Defect, Fault, and Yield Modeling, pp. 178-187, May 1995.

Examiner: Date Considered: 8/3/05

EXAMINER: Initial if reference considered, whether nor not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.